

DANIEL N. PALEY

DANIEL@DANIELPALEY.COM

650 - 868 - 9014

SUMMARY	<p>More than 20 years in hardware/ASIC/IP design, hands on, architecture and verification experience. International project and team management. Expertise in RFID architectures and standards. Proven ability to perform and excel in diverse cultural environments as a participant and leader.</p>
PROFESSIONAL EXPERIENCE	<p>Director of System Engineering, Tagent Corporation 2006 – Present</p> <ul style="list-style-type: none">• Lead the creation and development of system operation, protocols, and system development.• Primary contact to industry standards organizations (such as EPC Global, ANSI, ISO, etc) for both hardware and software standards.• Managed Systems Group, providing reader expertise for both hardware and software solutions.• Technical contact and management of partner programs.• Managed system design tasks for both hardware and software. <p><i>Director of Software Engineering, Applied Wireless ID Group (AWID), CA 2005 – 2006</i></p> <ul style="list-style-type: none">• Developed and architected company's first product line of Software defined RFID Readers. Responsible for all aspects of the Tahoe program.• Worked with EPC Global (standards organization) to develop software standards. Co-Chair Application Level Events Working Group; Lead the CTE sub-committee of the Reader Operations Working group. Presented and lead technical discussions at both the general SAG meetings and Reader Operations meetings• Instrumental in the process of reaching consensus in setting the C1G2 specification. Worked with fellow members of the standards committee and staff of EPC Global.• Developed and maintained working relationship with partners and suppliers to keep development on schedule. Resolved problems with a positive outcome for all parties. <p><i>Director of Systems and Protocols, Intellex Corporation, CA 2004 – 2005</i></p> <ul style="list-style-type: none">• Developed and architected company's first product line of Class-3 RFID tags and systems. Authored several architecture specifications for the product line.• Worked with EPC Global to develop the Class-1 Generation-2 UHF RFID standard. Co-chair of Hardware Action Group Technical sub-committee. Presented at general HAG meeting the findings of the sub-committee.• Instrumental in the process of reaching consensus in setting the C1G2 specification. Worked with fellow members of the standards committee and staff of EPC Global.

519 GRAND STREET
REDWOOD CITY, CALIFORNIA 94062
PHONE 650 - 367 - 6819
CELL 650 - 868 - 9014
E-MAIL DANIEL@DANIELPALEY.COM

- Developed and maintained working relationship with partners and suppliers to keep development on schedule. Resolved problems with a positive outcome for all parties.

Contractor, Virtual-Silicon, Sunnyvale, CA. 2003

- Developed, architected, and verified three technology important test chips, completing the contract requirements on time.

Sr. ASIC Designer, Xerox Corporation, Impact Group, Palo Alto, CA. 1999 – 2002

- Successfully completed the architecture and design of the interconnect unit for the Image Processor project. This allowed up to 64 processors to be connected for increased processing power, allowing commands and data to be routed in the most optimal path possible.
- Initiated architectural design and implemented microcode of color conversion module in development of the MXP5800 Digital Media Processor chip. This processor was created in partnership with Intel.
- Initiated and lead the evaluation, research, and development of methodology tools responsible for improved internal and external communications. Devised a set of methodologies and tools, which allowed for creation and maintenance of products.
- Created a web and email based Bug/Issue tracking software package to follow onsite and offsite issues associated with all architecture, design and implementation.
- Developed standardized directory structure incorporating design repositories, testing, and code development for both hardware and software, which facilitated design reuse.

Principal Engineer, Manager, Project Lead., Phoenix Technologies Ltd., Virtual Chips Division, San Jose, CA. 1998 –1999

- Managed, led, architected, and designed the Multimedia Link core for 1394a (with MPEG and 61883 enhancements) project resulting in customer on time shipment of their product.
- Managed international engineering team. Provided leadership and training for all aspects of Test Environment product.
- Architected, designed, and developed Test Environment for 1394a project, which received a U.S. patent.
- Architected, designed, and developed Accelerated Graphics Port (AGP) Host Controller core. Managed design team to complete Host core using Verilog. Continued ongoing support with Applications, Sales, and Marketing.

Project Leader, Design and Verification Vadem. San Jose, CA. 1995 – 1996.

- Managed the successful completion of the VG330, an SOC microcontroller. Significantly improved existing verification for design and test for manufacturing

	<p><i>Member of Technical Staff, Rambus Inc., Mountain View, CA. 1991 – 1995.</i></p> <ul style="list-style-type: none"> • Initiated and led design verification of first-generation RDRAM product resulting in successful product launches and continued company success. • Verified and debugged RAC and RDRAM second-generation products for LSI and Nintendo projects in a condensed schedule time frame. • Initiated and designed video and computer interfaces of demonstration project that showcased the high-speed memory design. <p><i>Design Engineer, Olivetti Networks and Systems, Standard Platform Division, Menlo Park, CA. 1989 – 1991.</i></p> <ul style="list-style-type: none"> • Developed EISA design for I860 workstation in partnership with Microsoft. Implemented protocol design in a non-x86 architecture system. • Architected, and developed service processor board for minicomputer system, which allowed for real time data collection and system maintenance. • Implemented PLL Clock Chip for minicomputer system, which required less than 2ns of clock skew between all chips in the system. Completed this development from debug through tape out, and test vector generation. <p><i>Design Engineer, CAE Link Flight Simulator Corporation. (Formerly Singer Link Flight), Advanced Products Operations, Sunnyvale, CA. 1986 – 1989.</i></p> <ul style="list-style-type: none"> • Designed LANTIRN simulator project board one, which simulated different graphic views with symbology and text overlays. • Completed Priority Sectoring Processor of the Digital Image Generator. Implemented bug fixes in documentation and hardware both at onsite and offsite locations, which was critical in customer acceptance tests.
<p><u>EDUCATION</u></p>	<p>Bachelor of Science, Computer Engineering. University of the Pacific, Stockton, CA. May, 1986.</p>
<p><u>TOOLS</u></p>	<p>Verilog, Synopsys, Hspice, Python, Perl, C/C++, Assembly, PHP, HTML, MySQL, Unix, Linux, Windows, and others.</p>
<p><u>PATENTS</u></p>	<p>Patent Number: 6,457,152, Device and Method for testing a device through resolution of data into atomic operations. Granted Sept 24, 2002.</p> <p>10 additional patents filed in the area of RFID.</p>